forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film on the first conductive layer;

forming a second conductive layer on the first insulating film;

forming the control gate in stripes composed of the second conductive layer, the first insulating film in stripes and the floating gate in a rectangular solid composed of the first conductive layer by etching with a mask in stripes extending a direction perpendicular to the first conductive layer;

after said forming of the source/drain region, removing a portion of the tunnel oxide film immediately under part of the floating gate by isotropical etching; and

depositing a second insulating film on the control gate, sidewalls of the first insulating film, the floating gate and the tunnel oxide film to be covered with the second insulating film.

A4 cont'd

2. (Amended) A method for manufacturing a nonvolatile semiconductor memory wherein memory cells formed in a matrix on a semiconductor substrate wherein each memory cell comprises a tunnel oxide film, a floating gate, a first insulating film and a control gate stacked in this order, the method comprising:

forming the tunnel oxide film on the semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate on the tunnel oxide film;

patterning the first conductive layer in stripes extending in one direction;

forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film on the first conductive layer;

forming a second conductive layer on the first insulating film;

forming the control gate in stripes of the second conductive layer, the first insulating film in stripes and the floating gate in a rectangular solid of the first conductive layer by etching with a mask in stripes extending a direction perpendicular to the first conductive layer;

A4 cont'd

removing a portion of the tunnel oxide film immediately below a sidewall of the floating gate by isotropical etching;

depositing a second insulating film on the control gate, sidewalls of the first insulating film, the floating gate and the tunnel oxide film to be covered with the second insulating film; and

wherein after the second insulating film is deposited, thermal oxidation is performed to oxidize the sidewall of the floating gate via the second insulating film.

Please add the following new claims:

A5

5. (New) A method for manufacturing a nonvolatile semiconductor memory comprising at least one memory cell including a tunnel oxide film, a floating gate, a first insulating film and a control gate, the method comprising:

forming the tunnel oxide film so as to be supported by at least a semiconductor substrate;

forming a first conductive layer to be used as a material of the floating gate over the tunnel oxide film;

patterning the first conductive layer;

forming a source/drain region in a surface of the semiconductor substrate by using the first conductive layer as a mask;

forming the first insulating film over at least the first conductive layer;

forming a second conductive layer over at least the first insulating film, and patterning the second conductive layer to form at least one control gate;

after said forming of the source/drain region and after the floating gate has been formed via the first conductive layer, removing a portion of the tunnel oxide film immediately under part of the floating gate by etching; and

depositing a second insulating film over at least the control gate, at least one sidewall of the first insulating film, at least one sidewall of the floating gate and at least one sidewall of the tunnel oxide film.

6. (New) The method of claim 5, wherein after the second insulating film is deposited, thermal oxidation is performed to oxidize the sidewall of the floating gate via the second insulating film.

7. (New) The method of claim 5, wherein said etching used to remove the portion of the tunnel oxide film comprises isotropic etching by wet etching using at least a fluorinated acid.

A5 contd

8. (New) The method of claim 5, wherein the second insulating film comprises silicon oxide, and is formed via chemical vapor deposition.

REMARKS

This is in response to the Office Action dated March 12, 2003. New claims 5-8 have been added. Thus, claims 1-8 are now pending. Attached hereto is a marked-up version of the changes made to the specification and claim(s) by the current amendment. The attached page(s) is captioned "Version With Markings To Show Changes Made."

General

For purposes of example and without limitation, certain embodiments of this invention relate to a method of making a nonvolatile semiconductor memory including at least one memory cell. Figs. 3C and 4C illustrate an example memory cell including a tunnel oxide film 2, a floating gate 3, a first insulating film 7 (e.g., ONO), a control gate 8, and an overlying second insulating film 10. A relevant aspect of certain example embodiments of this invention is shown in Figs. 5A-5D, and relates to processing of the tunnel oxide film 2 after the source/drain regions 4, 5 have been formed.

In particular, after the source/drain regions 4, 5 have been formed (e.g., by ion implantation) using material of the floating gate 3 as a mask, the control gate 8 is formed.